WHAT IS CLAIMED IS:

1. A semiconductor package substrate having a contact pad protective layer formed thereon, comprising:

at least one insulating layer having a plurality of conductive blind vias formed therein and electrically connected to inner traces disposed underneath the insulating layer;

at least one patterned trace layer electroplated via a conductive film on the insulating layer, the patterned trace layer comprising a plurality of contact pads, wherein at least one of the contact pads is electrically connected to at least one of the blind vias; and

at least one metal barrier layer for covering the contact pads.

2. The semiconductor package substrate of claim 1, further comprising: a solder mask for covering the patterned trace layer and having a plurality of openings to expose the metal barrier layer.

3. The semiconductor package substrate of claim 1, wherein the substrate has a multi-layered structure having a plurality of non-conductive layers, and the insulating layer is one of the non-conductive layers formed closest to an outside-exposed surface of the substrate.

4. The semiconductor package substrate of claim 1, wherein the substrate is a flip-chip package substrate or a wire-bonded package substrate.

5. The semiconductor package substrate of claim 1, wherein the contact pad is selected from the group consisting of a bump solder pad, solder ball pad, and wire-bonded pad.

6. The semiconductor package substrate of claim 1, wherein the metal barrier layer is made of a material selected from the group consisting of gold (Au), nickel (Ni), palladium (Pd), silver (Ag), tin (Sn), Ni/Pd, chromium (Cr)/titanium (Ti), Ni/Au, Pd/Au, and Ni/Pd/Au.

7. A fabrication method for a semiconductor package substrate having a contact pad protective layer formed thereon, the method comprising the steps of:

providing an insulating layer having a plurality of blind vias formed therein for exposing inner traces disposed underneath the insulating layer;

forming a conductive film on the insulating layer and over the blind vias;

forming a first resist layer on the conductive film, wherein the first resist layer has a plurality of openings to expose predetermined parts of the conductive film;

performing a first electroplating process to form a patterned trace layer in the openings and in the blind vias to form conductive vias, wherein the patterned trace layer comprises a plurality of contact pads, and at least one of the contact pads is electrically connected to at least one of the conductive vias;

forming a second resist layer over the patterned trace layer exclusive of the contact pads, making the contact pads exposed from the second resist layer;

performing a second electroplating process to form a metal barrier layer on the contact pads; and

removing the second resist layer, the first resist layer, and parts of the conductive film covered by the first resist layer.

8. The fabrication method of claim 7, further comprising: a solder mask for covering the patterned trace layer and having a plurality of openings to expose the metal barrier layer.

9. The fabrication method of claim 7, wherein the substrate has a multi-layered structure having a plurality of non-conductive layers, and the insulating layer is one of the non-conductive layers formed closest to an outside-exposed surface of the substrate.

10. The fabrication method of claim 7, wherein the substrate is a flip-chip package substrate or a wire-bonded package substrate.

11. The fabrication method of claim 7, wherein the contact pad is selected from the group consisting of a bump solder pad, solder ball pad, and wire-bonded pad.

12. The fabrication method of claim 7, wherein the metal barrier layer is made of a material selected from the group consisting of gold (Au), nickel (Ni), palladium (Pd), silver (Ag), tin (Sn), Ni/Pd, chromium (Cr)/titanium (Ti), Ni/Au, Pd/Au, and Ni/Pd/Au.

13. The fabrication method of claim 7, wherein the first or second resist layer is a dry photoresist film or a liquid photoresist.

14. A fabrication method for a semiconductor package substrate having a contact pad protective layer formed thereon, comprising the steps of:

providing an insulating layer having a plurality of blind vias formed therein for exposing inner traces disposed underneath the insulating layer;

forming a conductive film on the insulating layer and over the blind vias;

forming a resist layer on the conductive film, the resist layer having a plurality of openings to expose predetermined parts of the conductive film;

performing a first electroplating process to form a plurality of contact pads in the openings and form a plurality of conductive vias in the blind vias, wherein at least one of the contact pads is electrically connected to at least one of the conductive vias;

performing a second electroplating process to form a metal barrier layer on the contact pads; and

removing the resist layer and parts of the conductive film covered by the resist layer.

15. The fabrication method of claim 14, further comprising: a solder mask formed on the substrate and having a plurality of openings to expose the metal barrier layer.

16. The fabrication method of claim 14, wherein the openings of the resist layer correspond in position to the blind vias of the insulating layer.

17. The fabrication method of claim 14, wherein the substrate has a multi-layered structure having a plurality of non-conductive layers, and the insulating layer is

one of the non-conductive layers formed closest to an outside-exposed surface of the substrate.

18. The fabrication method of claim 14, wherein the substrate is a flip-chip package substrate or a wire-bonded package substrate.

19. The fabrication method of claim 14, wherein the contact pad is selected from the group consisting of a bump solder pad, solder ball pad, and wire-bonded pad.

20. The fabrication method of claim 14, wherein the metal barrier layer is made of a material selected from the group consisting of gold (Au), nickel (Ni), palladium (Pd), silver (Ag), tin (Sn), Ni/Pd, chromium (Cr)/titanium (Ti), Ni/Au, Pd/Au, and Ni/Pd/Au.